We claim:

1. A digitally controlled circuit for reducing a phase modulation of a given signal, comprising:

a multiphase clock generator producing n phases of a clock being m-times the given signal;

a multiplexer connected to said multiphase clock generator and having n inputs for receiving the n phases of the clock, said multiplexer having one output supplying an output signal;

a phase comparator having inputs receiving the output signal of said multiplexer and the given signal, and generating a compared output signal; and

a sigma-delta modulator connected to said phase comparator and receiving said compared output signal, said sigma-delta modulator generating correction commands used for controlling said multiplexer.

2. The circuit according to claim 1, including a phase-difference accumulator and a phase-difference transformer connected to said difference accumulator, said phase-difference accumulator and said phase-difference transformer disposed between said phase comparator and said sigma-delta modulator.

3. The circuit according to claim 1, including a further sigma-delta modulator connected to said phase comparator and the given signal is supplied to an appropriate one of said inputs of said phase comparator through said further sigma-delta modulator for clock rate conversion.

4. The circuit according to claim 2, including an edge recognition circuit disposed between said multiplexer and said sigma-delta modulator, the correction commands of said sigma-delta modulator are supplied to said multiplexer through said edge recognition circuit, and said edge recognition circuit receives and is actuated by the output signal of said multiplexer.

5. The circuit according to claim 4, including a divider circuit disposed between said multiplexer and said sigma-delta modulator, said divider circuit receiving the output signal from said multiplexer and generates an output signal received by and actuating said phase-difference accumulator and said signal-delta modulator.

6. The circuit according to claim 5, wherein said divider circuit has a division ratio corresponding to a ratio of the output signal to the given signal, if appropriate after a clock-rate conversion by said further sigma-delta modulator.

7. The circuit according to claim 1, wherein said sigma-delta modulator is a binary adder adding values coming from said phase comparator, and overflow and underflow outputs of said binary adder are used for producing the correction commands.

8. The circuit according to claim 2, wherein said phase-difference accumulator has a counter and a circuit for recognizing an overflow and an underflow of said phase comparator, said circuit has an output connected to said counter which counts upward for any overflow and downward for any underflow.

9. The circuit according to claim 1, wherein m is equal to four and n is equal to four.